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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/602,253	06/23/2003	Salman Akram	2269-3091.5US (96-0890.04)	1942
24247	7590	02/25/2005	EXAMINER	
TRASK BRITT P.O. BOX 2550 SALT LAKE CITY, UT 84110			ANDUJAR, LEONARDO	
			ART UNIT	PAPER NUMBER
			2826	

DATE MAILED: 02/25/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)
	10/602,253	AKRAM, SALMAN
	Examiner Leonardo Andújar	Art Unit 2826

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --
Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1) Responsive to communication(s) filed on 21 January 2005.
 2a) This action is FINAL. 2b) This action is non-final.
 3) Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4) Claim(s) 1-15 is/are pending in the application.
 4a) Of the above claim(s) 5 and 12 is/are withdrawn from consideration.
 5) Claim(s) _____ is/are allowed.
 6) Claim(s) 1-4, 6-11 and 13-15 is/are rejected.
 7) Claim(s) _____ is/are objected to.
 8) Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9) The specification is objected to by the Examiner.
 10) The drawing(s) filed on _____ is/are: a) accepted or b) objected to by the Examiner.
 Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
 Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
 11) The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12) Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
 a) All b) Some * c) None of:
 1. Certified copies of the priority documents have been received.
 2. Certified copies of the priority documents have been received in Application No. _____.
 3. Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) Notice of References Cited (PTO-892)
 2) Notice of Draftsperson's Patent Drawing Review (PTO-948)
 3) Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)
 Paper No(s)/Mail Date _____

4) Interview Summary (PTO-413)
 Paper No(s)/Mail Date. _____

5) Notice of Informal Patent Application (PTO-152)
 6) Other: _____

DETAILED ACTION

Continued Examination Under 37 CFR 1.114

1. A request for continued examination under 37 CFR 1.114, including the fee set forth in 37 CFR 1.17(e), was filed in this application after final rejection. Since this application is eligible for continued examination under 37 CFR 1.114, and the fee set forth in 37 CFR 1.17(e) has been timely paid, the finality of the previous Office action has been withdrawn pursuant to 37 CFR 1.114. Applicant's submission filed on 11/26/2004 has been entered.

Election/Restrictions

2. Applicant's election without traverse of species 1 in a communication filed on 02/23/2004 is acknowledged. New claim 12 has been withdrawn from further consideration since it is directed to a non-elected species 4.

Priority

3. An application in which the benefits of an earlier application are desired must contain a specific reference to the prior application(s) in the first sentence of the specification or in an application data sheet (37 CFR 1.78(a)(2) and (a)(5)). The specific reference to any prior nonprovisional application must include the relationship (i.e., continuation, divisional, or continuation-in-part) between the applications except when the reference is to a prior application of a CPA assigned the same application number.

Claim Rejections - 35 USC § 103

4. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

5. Claims 1-4, 6-11 and 13-15 are rejected under 35 U.S.C. 103(a) as being unpatentable over Duboz et al. (US 5,726,500) in view of Schaefer et al. (US 6,075,290) further in view of Elenius et al. (US 6,441,487).

6. Regarding claim 1, Duboz (e.g. fig. 5) shows most aspects of the instant invention including a semiconductor substrate 51; a passivation layer (not labeled) and a metal connection 58 formed in the passivation layer which has been sized and configured to temporarily establish an electrical connecting (inherent) by way of biased contact against a substantially spherical interconnection element 67 attached to a semiconductor device 30. Duboz, also, shows an external electrode 36 overlapping the electrodes 69. It is inherent that this type of connection is temporally since an In connection can be detached by the use of heat.

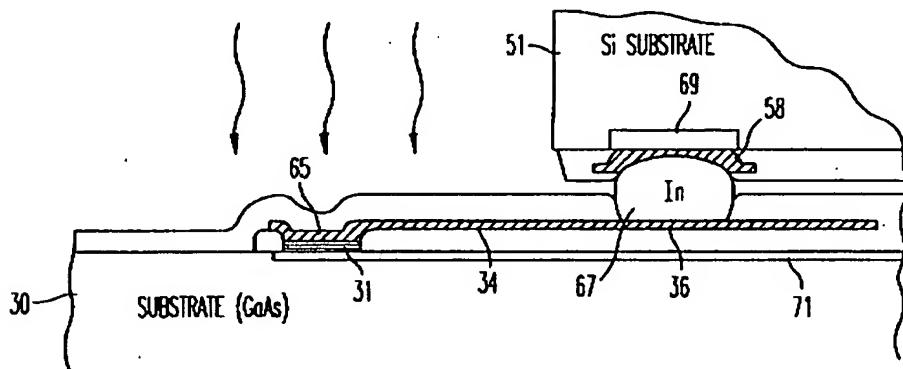
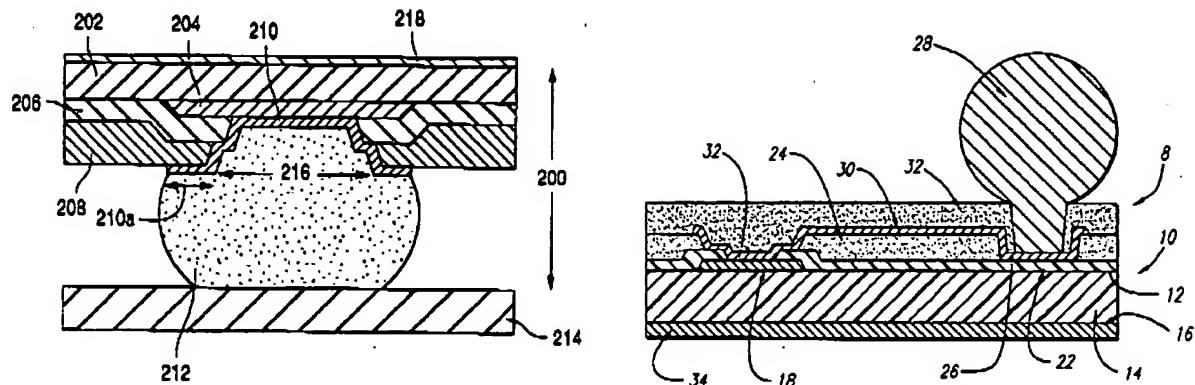


FIG. 5

Duboz does not show that the metal connection is a metal lined via formed in the passivation layer or a conductive trace overlapping a dielectric layer. Nevertheless, Schaefer shows a metal lined via 210 in a passivation layer 206/208 whereas Elenius (e.g. fig. 2) shows a conductive trace 30 on a dielectric layer 22 and a passivation layer 24 over the conductive trace. The metal lined vias according to Schaefer's invention prevent stress related problems such as crack formations within the die (see Schaefer's fig. 2, col. 2/lls. 32-67; col. 3/lls. 1-11 & col. 5/lls. 41-44). Elenius' embodiment provides an improved chip scale package that has a small form factor, i.e. the resulting chip scale package is not larger than the size of the original integrated circuit (col. 3/lls. 16-41). Furthermore, Elenius discloses that the size and the amount of the solder bumps are compromised due to the fact that the solder pads are typically located at the perimeter of the integrated circuit. The solder bump contact pads can be redistributed internally, away from the outer perimeter of the integrated circuit; the size of such solder bumps is unchanged. Therefore, the requirements of complex integrated circuits can be fulfilled (col. 2/lls. 25-40). Additionally, both connections are configured to temporally establish an electrical connection. It is inherent that this type of connection is temporally since a solder connection can be detached by the use of heat (see Brillhart; teaching reference).



It would have been obvious to one of ordinary skill in the art at the time the invention was made to make Duboz's metal connection in form of metal lined via to prevent stress related problems such as craze formations within the die as taught by Schaefer and to provide the a conductive trace over a dielectric layer in Duboz in view of Schaefer's invention in order to improved the chip scale package by providing a small form factor, i.e. the resulting chip scale package is not larger than the size of the original integrated circuit, and to internally redistribute the solder bump contact pads, away from the outer perimeter of the integrated circuit to fulfill the requirements of complex integrated circuit as taught by as taught by Elenius.

7. Regarding claims 2 and 3, Duboz in view of Schaefer further in view of Elenius teaches that the metal lined via is formed of a size and shape to receive approximately less than the 50% of an overall height of a substantially spherical interconnection element 212 (see Schaefer's fig. 2). Duboz in view of Schaefer further in view of Elenius does not explicitly disclose specific values such as 30% or between 10 and 50 % of the overall height of the interconnection element 212. Nevertheless, a change in size is

generally recognized as being within the level of ordinary skill in the art. *In re Rose*, 105 USPQ 237 (CCPA 1955). It would have been an obvious matter of design choice to make the lined via having a size of approximately 30% or between 10 and 50% of the overall height of the interconnection element 212, since such a modification would have involved a mere change in the size of a component as taught by *In re Rose*, 105 USPQ 237 (CCPA 1955).

8. Regarding claim 4, Schaefer shows that the via includes sloped sidewalls.
9. Regarding claim 6, Elenius shows that the conductive traces includes copper (col. 7/lls. 1-28).
10. Regarding claim 7, Elenius shows that the passivation layer comprises polyimide (col. 6/ll. 45).
11. Regarding claim 8, Schaefer in view of Elenius discloses the claimed invention except for metal lined via comprising a material from the group of gold, platinum, and tungsten. It would have been obvious to one having ordinary skill in the art at the time the invention was made to metal lined via disclosed by Shafer in view of Elenius comprising a material from the group of gold, platinum, and tungsten, since it has been held to be within the general skill of a worker in the art to select a known material on the basis of its suitability for the intended use as a matter of obvious design choice. *In re Leshin*, 125 USPQ 416.
12. Regarding claim 9, Elenius does not explicitly teach that the dielectric layer 22 is made of silicon oxide. However, Elenius teaches that the dielectric layer 22 is a passivation layer whereas Schaefer teaches that passivation may comprise insulating

materials such as silicon oxide (col. 5/llls. 61-63). Furthermore, it has been held to be within the general skill of a worker in the art to select a known material on the basis of its suitability for the intended use as a matter of obvious design choice. *In re Leshin*, 125 USPQ 416. It would have been obvious to one having ordinary skill in the art at the time the invention was made to make the insulating layer disclosed by Duboz in view of Schafer further in view of Elenius of silicon oxide because Schaefer teaches that insulating layers such as passivation layers can be made of silicon oxide and because it has been held to be within the general skill of a worker in the art to select a known material (i.e. silicon oxide) on the basis of its suitability for the intended use (i.e. passivation layer) as a matter of obvious design choice as taught *In re Leshin*, 125 USPQ 416.

13. Regarding claims 10 and 11, Duboz in view of Schaefer further in view of Elenius shows most aspects of the instant invention except for a passivation layer having a thickness of about 20-25 or about 100 microns. However, the specification contains no disclosure of either the critical nature of the claimed arrangement or any unexpected results arising therefrom. Where patentability is said to be based upon particular chosen dimensions or upon another variable recited in a claim, the applicant must show that the chosen dimensions are critical. *In re Woodruff*, 919 F.2d 1575, 1578, 16 USPQ2d 1934, 1936 (Fed. Cir. 1990). Additionally, a change in size is generally recognized as being within the level of ordinary skill in the art. *In re Rose*, 105 USPQ 237 (CCPA 1955). It would have been an obvious matter of design choice to make the passivation layer having a thickness of about 20-25 or 100 micros since such a modification would have

involved a mere change in the size of a component as taught by *In re Rose*, 105 USPQ 237 (CCPA 1955).

14. Regarding claims 13-15, Duboz in view of Schaefer further in view of Elenius shows that the metal lined via is sized and configured to temporary establish the electrical connection comprising discrete interconnection at a plurality of contact lines circling the substantially spherical interconnection element.

Response to Arguments

15. Applicant's arguments filed 11/29/2004 have been fully considered but they are not persuasive.

16. In response to applicant's arguments against the references individually, one cannot show nonobviousness by attacking references individually where the rejections are based on combinations of references. See *In re Keller*, 642 F.2d 413, 208 USPQ 871 (CCPA 1981); *In re Merck & Co.*, 800 F.2d 1091, 231 USPQ 375 (Fed. Cir. 1986).

17. Applicant argues that the new added limitation is not taught by the prior art. Initially, it is respectfully noted that "new added limitation" is considered functional language. Any functional language must result in a structural difference between the claimed invention and the prior art in order to patentably distinguish the claimed invention from the prior art. If the prior art structure is capable of performing the intended use, then it meets the claim. In a claim drawn to a process of making, the intended use must result in a manipulative difference as compared to the prior art. *In re Casey*, 152 USPQ 235 (CCPA 1967); *In re Otto*, 136 USPQ 458, 459 (CCPA 1963).

Furthermore, this limitation is implicit in the teaching of Duboz since in this type of detector a biased communication exists between the substrate and the chip. As is known in the electronic art this communication is obtained by temporary electrical connection. Also, Duboz (e.g. fig. 5) shows that the metal connection 58 is configured to temporally establish an electrical connection by way of biased contact against a substantially spherical interconnection element 67 attached to a semiconductor device 30 (inherent). The fact that the connections are soldered does not imply that the connection is not configured to temporally establish an electrical connection by way of biased contact against a substantially spherical interconnection. Furthermore, it is known in the art this type of solder connection (i.e. flip chip) is not permanent because they must provide the capability of being detached. Usually, defective flip chips are replaced after being tested. One of the advantageously properties of the solder material is its reworkability. As evidenced by Brillhart (teaching reference) it is known in the art that a solder connection can be detached by heat application (col. 3/lls. 44-54). Therefore, it is respectfully noted that this type of solder connection is a temporally connection.

18. Furthermore, there is not indication in Schaefer that the stress related detriments that are taught by Schaefer is due to the melting and bonding of the contact bump as suggested by Applicant. On the other hand, what it is taught by Schaefer is that the problem is caused by a difference between the coefficient of thermal expansion (CTE) of the chip and the CTE of substrate. In that regards, it is inherent that that there is a difference in CTE between the chip and the substrate disclosed by Duboz. The

examiner disagrees with applicant conclusion that this problem is only due to relative high temperature environment during the bonding process. Applicant ignored the fact that this problem also occurs during the entire device operational life due to the heat generated during operation. In any case, applicant fails to proof or to provide evidence that this phenomena does not occur at all in Duboz' device. If a *prima facie* case of obviousness is established, the burden shifts to the applicant to come forward with arguments and/or evidence to rebut the *prima facie* case. See, e.g., Dillon, 919 F.2d at 692, 16 USPQ2d at 1901. Rebuttal evidence and arguments can be presented in the specification, *In re Soni*, 54 F.3d 746, 750, 34 USPQ2d 1684, 1687 (Fed. Cir. 1995), by counsel, *In re Chu*, 66 F.3d 292, 299, 36 USPQ2d 1089, 1094-95 (Fed. Cir. 1995), or by way of an affidavit or declaration under 37 CFR 1.132, e.g., Soni, 54 F.3d at 750, 34 USPQ2d at 1687; *In re Piasecki*, 745 F.2d 1468, 1474, 223 USPQ 785, 789-90 (Fed. Cir. 1984). However, arguments of counsel cannot take the place of factually supported objective evidence. See, e.g., *In re Huang*, 100 F.3d 135, 139-40, 40 USPQ2d 1685, 1689 (Fed. Cir. 1996); *In re De Blauwe*, 736 F.2d 699, 705, 222 USPQ 191, 196 (Fed. Cir. 1984).

19. Applicant argues the references teaches and suggest interconnection structures specifically suited for incongruous or generally opposite thermal stress. Also, applicant argues that Duboz does not teach or suggest that its interconnection structure is suitable for the increases in temperature to which Schaefer is directed. Nevertheless, the test for obviousness is not whether the features of a secondary reference may be bodily incorporated into the structure of the primary reference; nor is it that the claimed

invention must be expressly suggested in any one or all of the references. Rather, the test is what the combined teachings of the references would have suggested to those of ordinary skill in the art. See *In re Keller*, 642 F.2d 413, 208 USPQ 871 (CCPA 1981). If a prima facie case of obviousness is established, the burden shifts to the applicant to come forward with arguments and/or evidence to rebut the prima facie case. However, arguments of counsel cannot take the place of factually supported objective evidence (see comments above). In this case, it seems irrelevant if the device disclosed by Duboz may be exposed to solder bonding temperatures or not because the interconnections disclosed by Duboz are made of indium. As it is known in the art, indium bumps can be interconnected at low temperature. If a prima facie case of obviousness is established, the burden shifts to the applicant to come forward with arguments and/or evidence to rebut the prima facie case. However, arguments of counsel cannot take the place of factually supported objective evidence (see comments above).

20. Applicant argues the presented modification may render each of the disparate structures unsatisfactory for its intended purpose and may interfere with a capability of Duboz structure to resist thermal stress due to decreases in temperature and vice versa. Nevertheless, the test for obviousness is not whether the features of a secondary reference may be bodily incorporated into the structure of the primary reference; nor is it that the claimed invention must be expressly suggested in any one or all of the references. Rather, the test is what the combined teachings of the references would have suggested to those of ordinary skill in the art. See *In re Keller*, 642 F.2d

413, 208 USPQ 871 (CCPA 1981). In this case, the secondary reference was used only to show that the missing limitation (a metal lined) is known in the art.

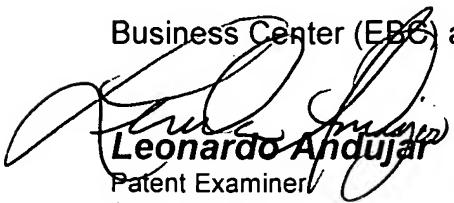
21. Applicant argues that since the device disclosed by Duboz operates at low temperature is suited for the stress associated with a reduction in temperature. Nevertheless, this fact does not imply that there is not stress introduced on the contact bump due to a difference in CTE.

Conclusion

22. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Leonardo Andújar whose telephone number is 571-272-1912. The examiner can normally be reached on Mon through Thu from 9:00 AM to 7:30 PM EST.

23. If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Nathan J. Flynn can be reached on 571-272-1915. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

24. Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).



Leonardo Andújar
Patent Examiner
Art Unit 2826
02/15/2005